

WHAT IS CLAIMED IS:

1. A charging circuit for charging a prescribed load circuit to a prescribed potential, the charging circuit comprising:

a charging driving circuit connected to the load circuit for supplying a charging signal to the load circuit from an output end of the charging driving circuit;

a time constant circuit for receiving the charging signal, changing a time constant of the charging signal and outputting a transition signal having a prescribed transition time period;

a control circuit for outputting a control signal for setting a time constant of the time constant circuit in accordance with the prescribed load circuit;

a voltage detection circuit for detecting that the transition signal output from the time constant circuit has reached the prescribed potential and outputting a detection signal; and

a delay and inversion circuit for delaying, and inverting a logic level of, an externally input charging control signal, and outputting a delay signal,

wherein the charging driving circuit starts a charging operation in accordance with the delay signal

output from the delay and inversion circuit, and terminates the charging operation in accordance with the detection signal output from the voltage detection circuit.

2. A charging circuit according to claim 1, wherein the output end is grounded by the delay signal during a delay time period from the time when the charging control signal is input to the delay and inversion circuit until the time when the delay signal is output.

3. A charging circuit according to claim 1, wherein:

an output section of the voltage detection circuit is a transfer gate which becomes conductive when the delay signal is placed into an active state,

the transfer gate is connected to a gate of a P-type MOS transistor of the charging driving circuit, and

the gate of the P-type MOS transistor is connected to a pull-up circuit for placing the P-type MOS transistor into a non-conductive state when the delay signal is placed into an inactive state.

4. A charging circuit according to claim 1, wherein:

the time constant circuit includes a plurality of P-type MOS transistors connected in series, and a plurality

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of N-type MOS transistors each having a source connected to a source of a respective P-type MOS transistor and a drain connected to a drain of the respective P-type MOS transistor,

a gate of each of the plurality of P-type MOS transistors is connected to ground,

a well region of each gate is connected to a prescribed internal power supply of the charging circuit, and

a gate of each of the plurality of N-type MOS transistors receives a control signal output from the control circuit.

5. A charging circuit according to claim 4, wherein an ON resistance of each of the plurality of N-type MOS transistors is set to be smaller than an ON resistance of each of the plurality of P-type MOS transistors.

6. A semiconductor memory device, comprising:

a charging circuit according to claim 1;

a pair of complementary bit lines connected to a memory cell; and

an equalizing circuit for equalizing the pair of complementary bit lines to an equal prescribed potential

using an equalizing signal acting as a charging control signal,

wherein an output end of the charging driving circuit of the charging circuit is connected to the pair of complementary bit lines.

7. A semiconductor memory device according to claim 6, comprising at least one more pair of complementary bit lines, wherein the output end of the charging driving circuit of the charging circuit is connected to the pairs of complementary bit lines.

8. A semiconductor memory device according to claim 6, wherein the equalizing circuit includes a pull-up circuit for charging the pair of complementary bit lines to a prescribed potential.

9. A semiconductor memory device according to claim 6, wherein the equalizing circuit includes a pull-up circuit for charging the pair of complementary bit lines to a prescribed potential, and the delay and inversion circuit of the charging circuit provides a delay time period which is at least equal to a time period required for the pair of complementary bit lines, charged to the prescribed

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potential by the pull-up circuit, to be discharged via the output end of the charging driving circuit.

10. A semiconductor memory device according to claim 8, wherein the delay and inversion circuit of the charging circuit provides a delay time period which is at least equal to a time period required for the pair of complementary bit lines, charged to the prescribed potential by the pull-up circuit, to be discharged via the output end of the charging driving circuit.